AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A square root extraction circuit for calculating binary input data $(0.a(1)) a(2) a(3) \ldots a(n))$ using a square root extraction algorithm to output binary square root data $(0.q(1) q(2) q(3) \ldots q(m))$, said square root extraction algorithm including an algorithm for determining said square root data on the basis of said input data by only additions of square root partial data $q(l)$ to $q(m)$ in $q(l)$ to $q(m)$ order, said square root extraction circuit comprising:

first to mth digit calculating portions each including a plurality of adders connected in series to that carries are propagated therethrough, wherein respective ones of said adders which are connected in the last position in said first to mth digit calculating portions provide carry outputs serving as said square root partial data $q(l)$ to $q(m)$, respectively, in accordance with said square root extraction ~~algorithm~~ algorithm,

wherein said plurality of adders include only a half adder and a full adder, and said full adder obtains only one bit of addition output and one bit of carry output based only on two bits of data input and one bit of carry input.

Claims 2-12 (Canceled)